WHAT IS CLAIMED IS:

1. A method for forming on a silicon substrate a non-volatile memory cell in an array region and a transistor in a region peripheral to the array region, the method comprising:

forming a polysilicon gate stack in the array region, and a transistor polysilicon gate in the peripheral region;

forming one of LDD and DDD regions in one or both source and drain regions of the transistor;

forming a spacer along one or more side-walls of each of the cell gate stack and the transistor gate;

forming an oxide layer over the spacers, the cell gate stack, and the transistor gate;

forming a highly doped region in each of said one of the LDD and DDD regions, wherein a lateral distance between an outer edge of the highly doped diffusion region and an outer edge of a corresponding one of LDD and DDD regions is dependent at least on a thickness of the oxide layer;

defining a contact hole area over one or both drain and source regions of the memory cell using a masking layer, wherein the contact area abuts or overlaps the polysilicon stack; and

performing a contact etch to form a contact hole in the contact hole area, wherein the spacer is substantially resistant to the contact etch.

2. The method of claim 1 further comprising:

before the oxide layer forming act, forming a sacrificial layer over the spacers, the cell gate stack, and the transistor gate.

3. The method of claim 2 wherein the spacer and the sacrificial layer comprise nitride.

4. The method of claim 2 wherein the contact etch removes the oxide layer and part or all of the sacrificial layer.

5. The method of claim 1 wherein the one of LDD and DDD regions forming act is carried out after the spacer forming act but before the oxide layer forming act.

6. The method of claim 1 wherein the spacer is insulated from the side-walls of polysilicon layers in the gate stack.

7. The method of claim 1 further comprising:

forming an HTO layer over the gate stack to insulate the gate stack from the spacer.

8. The method of claim 7 further comprising:

forming the source and drain regions of the memory cell after the HTO layer forming act.

9. The method of claim 1 further comprising:

prior to the highly doped region forming act, performing an oxide etch to remove at least portions of the oxide layer over the drain and source regions of the transistor.

10. The method of claim 1 further comprising:

prior to the spacer forming act, forming a DDD region in the source or drain region of the cell; and

after the spacer forming act, forming a highly doped region in the DDD region.

11. The method of claim 1 wherein the memory cell is one of a split-gate cell and an ETOX stacked-gate cell.

12. A device comprising a non-volatile memory cell transistor in an array region and a transistor in a region peripheral to the array region, the device comprising:

a plurality of gate layers formed in the memory array, comprising a control gate and a floating gate of the memory cell transistor;

a gate layer of the peripheral transistor;

etch resistant spacers adjacent to the lateral edges of the gate layers in the memory cell transistor and the gate layer of the peripheral transistor;

first drain and source regions of the peripheral transistor, wherein the first drain and source regions are formed subsequent to the formation of an oxide layer; and

a conductive contact deposited in a contact hole formed adjacent to one of the etch resistant spacers in the memory cell transistor that contacts a drain or source region of

the memory cell transistor, wherein the oxide layer is etched away before the conductive contact is formed and the conductive contact abuts or overlaps the gate layers of the memory cell transistor.

13. The device of claim 12 wherein the etch resistant spacers are formed of nitride.

14. The device of claim 13 wherein a sacrificial nitride layer deposited on the nitride spacers is etched before the conductive contacts are formed.

15. The device of claim 12 wherein the gate layers in the memory array comprise first and second polysilicon layers.

16. The device of claim 12 wherein at least some of the peripheral transistors comprise low doped drain regions.

17. The device of claim 12 wherein at least some of the peripheral transistors comprise double doped drain regions.

18. A method for forming a non-volatile memory cell transistor in a memory array and a transistor in a region peripheral to the memory array, the method comprising:

forming a plurality of gate layers on a semiconductor region;

forming first spacers adjacent to the gate layers in the memory array and the transistor in the peripheral region;

forming an oxide film over the first spacers;

forming drain and source diffusion regions in the peripheral transistor;

masking and etching the oxide film to form a contact hole to a drain or source region of the memory array transistor, wherein the first spacers are substantially resistant to the contact hole etch; and

depositing a conductive layer on the memory cell transistor to form a contact to the drain or source region of the memory cell transistor, wherein the contact does not electrically connect to the gate layers of the memory cell transistor.

19. The method of claim 18 further comprising:

depositing a high thermal oxide film over the gate layers before the deposition of the first etch resistant spacers.

20. The method of claim 18 further comprising:

etching the oxide film prior to forming said drain and source diffusion regions in the peripheral region transistors to remove a portion of the oxide film adjacent to the semiconductor region.

21. The method of claim 18 wherein the first spacers are formed by depositing and etching a nitride layer, wherein the nitride layer is substantially resistant to the contact hole etch.

22. The method of claim 18 further comprising:

depositing a nitride layer over the first spacers, after forming the first spacers.

23. The method of claim 22 wherein portions of the nitride film are removed during the contact hole etch.

24. The method of claim 18 wherein the first spacers have a width between 100-700 angstroms.

25. The method of claim 18 further comprising:

forming a low doped drain region in the peripheral transistor before forming the first spacers adjacent to the gate layers.

26. The method of claim 18 further comprising:

forming a double doped drain region in the peripheral transistor before forming the first spacers adjacent to the gate layers.

27. The method of claim 18 wherein said drain and source diffusion regions in the peripheral transistor are formed by depositing a first concentration of dopants within second drain and source diffusion regions in the peripheral transistor that are doped with a second concentration of dopants lower than the first concentration of dopants.

28. A method for forming a device comprising a plurality of transistors in a flash memory array and a plurality of transistors in a peripheral region, the method comprising:

forming a plurality of gate layers on a semiconductor region;

forming first spacers adjacent to the gate layers of the transistors in the flash memory array and the transistors in the peripheral region;

depositing a second film over the first spacers;

depositing an oxide film over the second film;

forming drain and source diffusion regions in the peripheral region transistors; and

masking and etching the oxide film to form contact holes to drain or source regions of the memory array transistors,

wherein the first spacers and the second film are substantially resistant to the contact hole etch, and the first spacers insulate lateral walls of the gate layers in the memory array transistors subsequent to the contact hole etch.

29. The method of claim 28 further comprising:

depositing a high thermal oxide film over the gate layers before the formation of the first spacers.

30. The method of claim 28 further comprising:

etching the oxide film prior to forming said drain and source diffusion regions in the peripheral region transistors to remove a portion of the oxide film adjacent to the semiconductor region.

31. The method of claim 28 wherein the first spacers are formed by depositing and etching a nitride layer, wherein the nitride layer is substantially resistant to the contact hole etch.

32. The method of claim 28 wherein the second film is formed by depositing a nitride layer.

33 . The method of claim 32 wherein portions of the second are removed during the contact hole etch.

34. The method of claim 28 wherein the first spacers are between 100-700 angstroms wide.

35. A method for forming a non-volatile memory cell transistor in a memory array and a transistor in a region peripheral to the memory array, the method comprising:

forming a plurality of gate layers on a semiconductor region;

forming first spacers adjacent to the gate layers of the memory cell transistor and the transistor in the peripheral region;

depositing a second film over the first spacers;

depositing a first oxide film over the second film;

forming first drain and source diffusion regions in the peripheral region transistor;

depositing a second oxide film over the first oxide film;

forming second drain and source diffusion regions the peripheral region transistor; and

masking and etching the first and second oxide films to form contact holes to drain or source regions of the peripheral and memory array transistors,

wherein the first spacers and the second film are substantially resistant to the contact hole etch, and the first spacers insulate lateral walls of the gate layers in the memory array transistors and the peripheral region transistors subsequent to the contact hole etch.